In particular, the Examiner states on page 2 of the Office Action that "nowhere in the original specification ***expressly*** support and define the negative limitations of 'unbonded substrate' and 'without forming an implanted barrier layer in the substrate' (emphasis added). Claims 20, 25, 41 ,49 51, 53 and 55 have been amended to remove the negative limitation of "without forming an implanted barrier layer in the substrate."

The M.P.E.P, in section 2173.05(i) discusses the rules regarding negative claim limitations. This section states that "a lack of literal basis in the specification for a negative limitation may not be sufficient to establish a *prima facie* case for lack of descriptive support." The written description requirement for a given claim can be met if the disclosure reasonably conveys to one skilled in the art that the inventor had possession of the subject matter in question. *Fujikawa v. Wattanasin*, 39 USPQ2d 1895, 1904 (Fed. Cir. 1996). Such disclosure, contrary to the Examiner's statement, need not be "express."

Applicant respectfully submits that the specification reasonably conveys that the Applicant had possession of the negative claim limitation of an "unbonded substrate" in Applicant's claims. The description of Applicant's claimed method begins on page 11, line 17 and continues to page 15, line 8, and references 13 different Figures, namely FIGS. 5A, 5B, 5C, 5D, 5E, 5F, 5G, 5H, 5I, 5J, 5K, 5L and 5M. It is manifestly clear from this description and from the numerous Figures that the inventors contemplated using a single, unbonded substrate. For example, the layers in Applicant's claimed invention are not and cannot be formed by interfacing separate substrates and then bonding them together, and then planarizing one of the substrates. Rather, the formation of each layer is described and illustrated as a separate act, which is characteristic of a method that employs a single substrate to form layered semiconductor device such as an array of memory cells.

Accordingly, Applicant respectfully submits that the remaining negative limitation in the claims concerning the "unbonded substrate" is supported in the written description of the specification and respectfully requests withdrawal of the rejection of the above-claims.

§102 Rejection of the Claims

Claims 20-21, 23-22, 27-28, 30, 32, 34-35, 37, 39, 41, 42, 44, 46, 48-53

Claims 20-21, 23-22, 27-28, 30, 32, 34-35, 37, 39, 41, 42, 44, 46, 48-53 were rejected under 35 USC § 102(b) as being anticipated by Gotou (U.S. 5,001,526).

Gotou is directed to forming a DRAM cell using so-called "bonded wafer" technology, as described in col 4, line 41 through col. 5, line 9 and FIGS. 4A, 4B and 5. This technology involves forming layers on two separate substrates, interfacing the substrates, bonding them together, and then polishing one of the substrates to obtain the multi-layered structure (FIG. 6).

Examiner continues to emphasize that Gotou includes a *single substrate* from which a number of access transistors are formed thereon. However, it is indisputable that the ***method*** taught in Gotou requires starting with and using ***two substrates*** and then ***bonding*** them together. This is in contrast to Applicant's claimed invention, which is a ***method*** that starts with and uses only a ***single unbonded substrate***. Applicant's claimed process does not include any method steps involving bonding substrates together to form the single substrate.

Applicant wishes to emphasize here that it is the ***specific acts making up the method*** that must be compared in determining whether a claimed invention is anticipated by a prior art reference. There must be no difference between the claimed invention and the reference disclosure, as viewed by one of ordinary skill in the art. *Scripps Clinic & Research Foundation v. Genentech, Inc.* 18 USPQ2d 1001, 1010 (Fed. Cir. 1991). The Examiner cannot omit or dismiss claim elements in performing the anticipation analysis; all the claim elements must be considered.

Applicant respectfully submits that when all of the acts in Applicant's method claims are given their due weight, they are not all found in Gotou, and in particular the "single unbonded substrate" limitation is not present in Gotou. Accordingly, Applicant traverses the anticipation rejection of the above-cited claims, and respectfully requests withdrawal of the rejection.

Claims 49-56

Claims 49-56 were rejected under 35 USC § 102(b) as being anticipated by Ho et al. (U.S.4,252,579) (hereinafter, "Ho"). Ho et al. discloses a method of making a single electrode metal-oxide-semiconductor field-effect transistor (MOSFET). The MOSFET includes electrical isolation areas (18) between openings (22), the latter being filled with doped polysilicon (26) to form a gate electrode. See col 5, lines 18-20 and FIGS. 3 and 4. The capacitor in the device is the depletion region (25) formed in the P- substrate surrounding the gate dielectric layer (24) and the electrode (26), as described in col. 5, line 47-51 and shown in FIG. 4.

As described in col. 6, lines 16-22, the method of forming the structure of Ho necessarily includes forming oxide trenches (16) and filling them with an insulating material to form isolation areas (18) between gate electrodes (26) (i.e., "potential wells") to reduce the noise coupling problem, i.e., the leakage of current between potential wells during the read operation.

In contrast, Applicant's claimed method invention does not include steps that involve forming such isolation areas. Accordingly, Applicant's claimed method invention cannot be said to be anticipated by the method of Ho. Applicant therefore respectfully requests the withdrawal of the anticipation rejection of the above-cited claims.

§103 Rejection of the Claims

Claims 20-21, 23-25, 27-28, 30, 32, 34, 35, 37, 39, 41-42, 44, 46, and 48-53

Claims 20-21, 23-25, 27-28, 30, 32, 34, 35, 37, 39, 41-42, 44, 46, and 48-53 were rejected under 35 USC § 103(a) as being unpatentable over Gotou taken with Joyner et al. (U.S.5,429,955) (hereinafter, "Joyner"). The teachings of Gotou has been described above.

Joyner teaches a method for constructing a semiconductor-on-insulator (SOI), i.e., a buried insulator layer in a wafer. A sacrificial layer (12) is formed on a semiconductor wafer (10) surface. The wafer is then subject to ion implantation to place ions (16) at predetermined depths below the wafer surface. During implantation, the sacrificial layer is gradually sputtered away, thereby compensating for the outgrowth of the silicon surface due to the volume of the implanted ions. A post-implant anneal is performed to allow the ions to react with the semiconductor to form a buried insulator (24).

The Examiner argues that the single SOI implanted substrate of Joyner could be used to modify the method of Gotou so that Gotou would not require using bonded substrate. However, the Applicant respectfully submits that this combination of references does not and cannot yield Applicant's claimed invention. Applicant's claimed invention does not included the oxide layer (13) of Gotou that would be somehow replaced by the buried insulating layer (24) of Joyner, so that alternate methods of forming oxide layer (13) are moot.

The fact remains that Applicant's claimed invention does not include the method steps set forth in Joyner, so that even if, *arguendo*, the methods of Joyner and Gotou could be somehow be combined (and Applicant notes with emphasis here that the Office Action does not address how this would be done), the added steps required by Joyner (e.g., forming a sacrificial layer, performing an ion implant, performing a post-implant anneal, etc.) are not part of Applicant's claimed invention.

Because the combination of the two cited references does not yield Applicant's invention, Applicant respectfully submits that a *prima facie* case for obviousness as to the above-cited claims has not been made, and therefore respectfully requests withdrawal of the rejection of the above-cited claims.

Claims 20, 29, 31, 32, 35, 38, 40, 43, 45, 47, 54-56

Claims 20, 29, 31, 32, 35, 38, 40, 43, 45, 47, 54-56 were rejected under 35 USC § 103(a) as being unpatentable over Gotou and Joyner as applied above, taken with Kimura et al. (5,177,576) (hereinafter, "Kimura").

Applicant notes here that it is not clear whether claim 26 was meant to be included in this rejection as well, though this claim is discussed in the Office Action on page 6, second through fourth paragraphs. Clarification is respectfully requested.

Applicant respectfully submits that the rejection of claims 20, 29, 31, 32, 35, 38, 40, 43, 45, 47, 54-56 (and claim 26, if applicable) is traversed for the reasons explained immediately above in connection with the obviousness rejection of claims 20-21, 23-25, 27-28, 30, 32, 34, 35, 37, 39, 41-42, 44, 46, and 48-53. Regardless of how the ***methods*** Gotou and Joyner would be combined, the result is a ***method*** that differs from Applicant's claimed ***method***.

Applicant therefore respectfully requests that the obviousness rejection under 35 USC § 103(a) of claims 20, 29, 31, 32, 35, 38, 40, 43, 45, 47, 54-56 be withdrawn.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Joseph Gortych at 802-660-7199, to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 22nd day of August, 2002.

Amy Moriarty
Name

_____
Signature